[Total No. of Questions - 8] [Total No. of Printed Pages - 3]
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M. Tech 1st Semester Examination

Design of Electronics System

EC-102

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : (i) Assume suitable data wherever necessary.

(ii) Attempt Any FIVE Questions.

1. (a) Explain the operation of flash type ADC with a suitable diagram. What are the limitations of this converter? Compare flash type ADC and successive approximation ADC in terms of accuracy, conversion speed and resolution. **(10)**

   (b) An analog voltage in the range of –V to + V is required to be converted into a 3-bit 2's complement digital format. The digital value for 0V should be 000 and the maximum quantization error should not exceed ± ½ LSB. Determine the quantization interval. **(5)**

   (c) How are signal assignment, variable assignment and constant declaration done in VHDL? **(5)**

2. (a) Design a BCD to Excess-3 code converter. Show all the necessary steps and K-maps. **(10)**

   (b) Draw and explain 4-bit magnitude comparator in detail. **(10)**

3. (a) What are the steps used for implementing combinational circuit using PLA? **(08)**

(b) How does architecture of PL A differ from ROM and PAL? **(6)**

(c) Specify the size of ROM that will accommodate the truth table for following combinational circuit components

(i) a binary multiplier that multiplies two 4-bit numbers

(ii) a 4-bit adder **(6)**

4. (a) Implement the following Boolean function with only one 4X I MUX

F (A, B, C, D) = Σ m (1, 3, 5, 7, 8, 11, 12, 15) **(10)**

(b) Write the design procedure for synchronous counter. Also design MOD-5 ripple counter. **(10)**

5. (a) Carry out the following conversion:

(i) Convert a D-latch to a JK

(ii) Convert D to SR **(10)**

(b) Draw and explain the clocked JK flip-flop in detail. Also Explain the RACE AROUND condition in flip-flop. What is remedy for this problem? **(10)**

6. (a) Draw and explain 4-bit universal shift register. **(8)**

(b) Analyze the sequential circuit as shown in Fig. 1. **(12)**

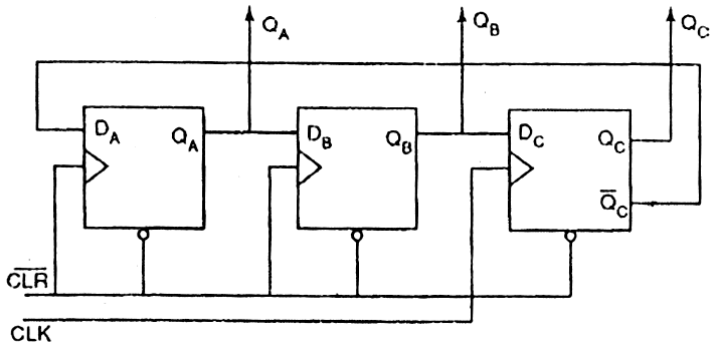

Fig. 1

7. (a) What do you mean by hazard free asynchronous sequential circuits. **(6)**

   (b) Define RACE in asynchronous sequential circuits. **(4)**

   (c) Implement the following function using PLA.

   $A(x,y,z) = \Sigma m\ (1,2,4,6)$

   $B(x,y,z) = \Sigma m\ (0,1,6,7)$

   $C(x,y,z) = \Sigma m(\ 2,6)$ **(10)**

8. (a) Design a synchronous counter with states 0, 1, 2, 3, 0, 1 using JK flip flops. **(8)**

   (b) Design a clocked sequential circuit using T-flip-flops for state diagram as shown in Fig. 2. Use state reduction if possible. Also use straight binary state assignment. **(12)**

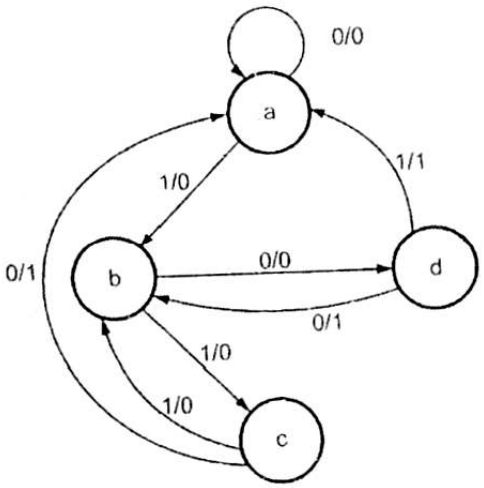

Fig. 2