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(2123)

1402

B. Tech 5th Semester Examination

Microprocessors (O.S.)

EC-5011

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Candidates are required to attempt five questions in all. Selecting one question from each of the sections A, B, C & D. Section E is compulsory.

SECTION - A

1. (a) What is a microprocessor? List the internal sections of a general purpose microprocessor and give the purpose and function of each section? **(8)**

   (b) What is system Bus? Give its role. **(6)**

   (c) Why does OP-code fetch cycle need 4T states although it is similar to memory read cycle. **(6)**

2. (a) Explain:

   (i) ALU (ii) Program counter (iii) Instruction Decoder **(6)**

   (b) Draw and explain the timing diagram of a memory. Write cycle of 8085 microprocessor. **(6)**

   (c) Differentiate between physical, logical and virtual memory. **(4)**

   (d) For each of the following pins of 8085 show whether it is an input line or output line and mention its function:

   (i) ALE (ii) HOLD (iii) READY (iv) SID **(4)**

SECTION - B

3. (a) Define OP-code, operand and mnemonics. Write the machine code for instruction MoV H, A, if opcode = 01, register code for A=$(111)_2$ and register code for H=$(100)_2$. **(6)**

   (b) Explain the different types of interrupt facilities available in 8085. **(8)**

   (c) Show what will happen if the following instructions are executed in 8085 micro-processor.

   MVI A, 10H

   SIM **(6)**

4. (a) Explain:

   (i) Vectored and non-vectored interrupts.

   (ii) Interrupt vector Table (IVT) and its significance. **(10)**

   (b) Explain, with the help of suitable schematic diagram, the interfacing of 2K RAM (Starting Address=2000H) and a 1K ROM (Starting Address=0000H) with 8085 microprocessor. **(10)**

SECTION - C

5. (a) Mention the various addressing modes in 8085 microprocessor with a corresponding example. **(8)**

   (b) Explain the following 8085 instructions:

   (i) DAA (ii) RAR (iii) RLC (iv) PCHL (v) CNC (vi) SHLD **(12)**

6. (a) Discuss the significance and function of Program Status Word (PSW) in 8085 microprocessor. **(6)**

   (b) For the instructions given below, how many memory operations (read/write) are to be performed during the execution in an 8085 microprocessor.

   (i) CALL 2000 H

   (ii) LDA 2000 H **(6)**

(c) The program and machine code for an 8085 microprocessor are given by:

3E	MVI A, C3
C3	
00	NoP
80	ADD B
3D	DEC A
C2	JNZ 800A
0A	
80	
C3	JMP 800C
0C	
80	
D3	OUT 10
10	
76	HLT

The Starting address of the above program is 7 FFFH. What would happen if it is executed from 8000H? **(8)**

SECTION - D

7. (a) List the operating modes of 8255 PPI. **(8)**

   (b) Specify handshake signals and their functions if port A of 8255A is setup as an output port in mode 1. **(6)**

   (c) What are the conditions to start 8253 timer? **(6)**

8. (a) Explain the operation of 8259 priority Interrupt controller with the help of suitable diagram. **(10)**

   (b) Explain master and slave mode of 8257 DMA controller with the help of suitable example. **(10)**

SECTION - E

9. (a) Name the different Hardware interrupts in 8085 microprocessor.

   (b) What do you mean by WAIT state? What is its need?

(c) Name a maskable, non-vectored & hardware interrupt in 8085 microprocessor.

(d) An 8085 MP is executing the program given below:

```
        MVI  A, 10H
        MVI  B, 10H
BACK:   NOP
        ADD B
        RLC
        JNC  BACK
        HLT
```

Find out how many times the operation NOP will be executed in the above mentioned program.

(e) Following program is executed in a 8085 microprocessor. Find out the number of instruction cycles it will take from START to HALT:

```
START :  MVI    A, 14H
SHIFT :  RLC
         JNZ    SHIFT
         HALT
```

(f) What are Tri-state devices and why are they essential in a Bus-oriented system?

(g) What is ALE? Explain the function of ALE in 8085.

(h) If the memory chip size is 256×1 bits, then find the number of chips required to make 1K bytes of memory.

(i) How many and which type of machine cycles are needed to cxecute PUSH PSW by an 8085 microprocessor?

(j) The following sequence of instructions are executed by an 8085 microprocessor:

```
1000    LXI SP, 27FFH
1003    CALL 1006H
1006    PoPH
```

What will be the content of stack pointer (SP) and HL register pair on completion of these instructions.

(2×10=20)