[Total No. of Questions - 9] [Total No. of Printed Pages - 3]
(2063)

824

B.Tech 4th Semester Examination

Computer Architecture

IT(ID)-4001

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt five questions in all selecting one question from each of sections A, B, C and D of question paper. Section E is compulsory.

SECTION - A

1. (a) Define computer architecture. Explain different technologies used for computer.

   (b) Explain details about measuring and reporting performance of any computer with suitable examples. **(5+10)**

2. (a) Discuss briefly about classifying instruction set architectures and operations in the instruction set.

   (b) Discuss briefly quantitative principles of computer design. **(5+10)**

SECTION - B

3. (a) How is pipelining implemented? What are major pipeline hazards?

(b) Explain the concepts and challenges of instruction-level parallelism. **(5+10)**

4. (a) What is MIPS R4000 pipeline?

(b) How to reduce branch costs with prediction? **(7+8)**

SECTION - C

5. (a) What is cache memory? What are procedures to protect memory?

(b) Discuss briefly about buses connecting I/O devices to CPU memory with suitable diagrams. Explain about RAID. **(5+10)**

6. (a) How to reduce in cache misses? Compare between cache memory and virtual memory.

(b) How to reduce hit time in main memory? What are procedures to reduce cache miss penalty? **(5+10)**

SECTION - D

7. (a) How to establish connection more than two computers? What are characteristics of applications domains of multi-processors?

(b) How to achieve synchronization in multiprocessors computer. Discuss about distributed shared memory architectures. **(7+8)**

8. (a) What are practical issues for commercial interconnection networks with suitable examples. How to establish connection the interconnection network media?

(b) Explain centralized shared memory architectures with suitable diagrams. What is simple network interconnections? **(7+8)**

SECTION - E

9. (a) Explain about various addressing modes.

(b) What is pipelining? How does it improve performance?

(c) Distinguish between RISC & CISC processor.

(d) Describe the structure of pipeline with an example.

(e) Explain various RAID levels.

(f) How the different types of hazards that arise in a pipeline can be rninimized?

(g) Explain the four-stage pipelining.

(h) What are Control hazards? Explain the techniques used to minimize control Hazards.

(i) Define cache memory. Explain any two mapping process followed in cache memory.

(j) Draw and explain the virtual memory organization. **(10×4=40)**