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(2063)

830

B.Tech 4th Semester Examination

Electronic Logic Circuit Design

EC-4003

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt five questions in all, selecting one question each from sections A, B, C and D. Section - E is compulsory.

SECTION - A

1. (a) Design a 4 bit binary to grey code converter.

   (b) Design a direct logic circuit to generate the sequences 100111 and 011101 simultaneously. **(10,10)**

2. (a) What do you mean by race around condition? How it is removed? Explain the working of positive edge triggered master-slave JK flip flop. Explain its excitation table.

   (b) Differentiate between synchronous and asynchronous circuits. Explain the various classifications of switching circuits. **(12,8)**

SECTION - B

3. (a) Draw a two input, two output synchronous sequential circuit which examines the input sequence in non- overlapping strings of three inputs each and produces a one output coincident with the last input of the string if and only if the string consisted of either 2 or 3 1's. Use S-R flip-flop in your realization.

   (b) What do you mean by the cascading of ripple counters? Design a 3-bit ripple counter. Explain the effects of propagation delay in ripple counters. For what minimum value of propagation delay in each FF will a 10-bit ripple counter skip a count when it is clocked at 10MHz. **(10,10)**

4. (a) Design a universal shift register with flip flops.

   (b) Design a JK counter that goes through states 2, 4, 5, 7, 9, 10, 12, 2, 4, 5..... Is the counter self- starting? Modify the circuit such that whenever it goes to any invalid state it comes back to state 2. **(10,10)**

SECTION - C

5. (a) A sequential circuit has two pulse inputs, x_1 and x_2. The output of the circuit becomes 1 when one or more consecutive x_1 pulses are followed by two x_2 pulses. The output then remains 1 for all subsequent x_2 pulses until an x_1 pulse occurs.

(a) Derive a minimal state table describing the circuit operation.

(b) Synthesize the circuit using set-reset flip-flops. **(20)**

6. A sequential circuit has two inputs x_1 and x_2 and two outputs z_1 and z_2, is to be designed so that z_1 (for i=1, 2) takes on the value 1 if and only if x_1 was the input that changed last.

(a) Find a minimum-row reduced flow table and a valid assignment.

(b) Assuming that all inputs are available in an uncomplemented as well as complemented form, show a realization using NAND gates. **(20)**

SECTION - D

7. Design a hazard free asynchronous sequential circuit with two input x1 and x2 and two outputs G and R, which is to behave in the following manner. Initially, both input and both outputs are equal to 0. Whenever G = 0 and either x1 or x2 becomes 1, G turns on i.e. becomes 1. When the second input becomes 1, R turns on. The first input that changes from 1 to 0 turns G off. R turns off when G is off and either input changes from 1 to 0. **(20)**

8. (a) Write a short note on hazards. Explain the methods to design hazard free combinational networks.

(b) What are types of decomposition? What are the conditions for serial and parallel decomposition? **(10,10)**

SECTION - E

9. (a) Realize the given T flip flop in such a way that it acts as a D flip flop.

(b) Convert a D-FF into JK-FF.

(c) Design a 3-bit ring counter.

(d) What are the limitations of finite state machine?

(e) Tabulate the excitation tables of JK and SR flip flop.

(f) With the help of example explain the term glitch.

(g) Write the following function in standard SOP

$F(x, y, z) = xy + z$

(h) What are pulse mode circuits?

(i) Write the differences between Mealy and Moore type machines.

(j) Explain the difference between latch and flip flop. **(2×10=20)**