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(2063)

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B. Tech 4th Semester Examination

Pulse Shaping and Wave Generation

EC-4005

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt five questions in all selecting one question each from sections A, B, C and D. Section - E is compulsory.

SECTION - A

1. (a) How low pass RC circuit act as integrator? Prove that an RC circuit behaves as a reasonably good integrator if RC > 15T, where T is the period of an input 'E_m sin ωt'.

   (b) Derive an expression for the rise time of the output of a high-pass circuit excited by a step input. Draw the response of a High pass circuit with small, medium and large time constants when input is square wave. **(10,10)**

2. (a) What is difference between high pass and low pass RL circuit? Establish the relation between:

   (i) Tilt and time constant in high pass RC circuit,

(ii) Rise time and time constant of low pass RC ckt.

Indicate clearly the assumption made.

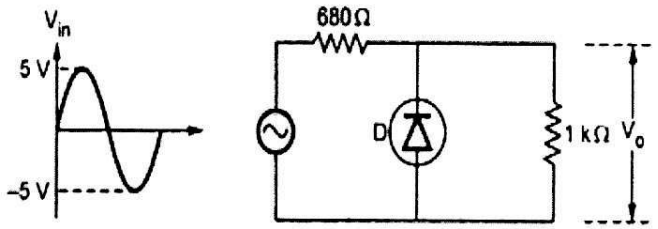
(b) Give the expression for rise time and fall time in terms of transistor parameters and operating currents.) **(10,10)**

SECTION - B

3. (a) Classify different types of clipper circuits. Give their circuits and explain their operation with the aid of transfer characteristics.

(b) State and prove clamping -circuit theorem,

(c) The limiter circuit is shown below:



Sketch its output waveform. **(10,5,5)**

4. (a) What is positive clamping and explain it with suitable circuit. Derive the relation between the tilts in the forward and reverse directions of the output of a clamping circuit excited by a square-wave input.

(b) Explain the terms pertaining to transistor switching characteristics.

i. Rise time and fall time.

ii. Delay time.

iii. Turn-on time.

iv. Storage time.

v. Turn-off time. **(10,10)**

SECTION - C

5. (a) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL gate with this.

   (b) Verify the truth table of RTL NOR gate with the circuit diagram of three inputs. **(10,10)**

6. (a) Why NAND and NOR are known as universal gates. Design a circuit which give high output when any of the two inputs are high.

   (b) With the help of circuit diagram explain the purpose of clamping diode in a positive diode AND gate. Describe the various characteristics of the logic family. **(10,10)**

SECTION - D

7. (a) Draw the circuit of the gated astable multivibrator and explain how it works?

   (b) Derive the expression for the gate width of a monostabie multivibrator considering the effect of reverse saturation current. What type of triggering is used in a monostabie multivibrator? Draw the circuit of it. **(10,10)**

8. (a) Explain the working of unidirectional diode gate. What are the advantages of unidirectional sampling gates?

(b) Why are sampling gates called Selection circuits? Compare the unidirectional and bi directional sampling gates. **(10,10)**

SECTION - E

9. (i) What is sampling gate? Explain how it differ from Logic gates?

(ii) Draw response of high pass RC circuit to ramp waveform.

(iii) What are Fan out, fan in, and noise immunity?

(iv) What are the drawbacks of two diode sampling gate?

(v) What do understand by dynamic analysis of switches?

(vi) Define a diode forward recovery time and reverse recovery time.

(vii) What is wired logic.

(viii) What the factors that contribute the delay time of transistor switch?

(ix) Draw a circuit to transmit that part of a sine wave which lies between +4V and +8V.

(x) Explain the variation of VBE(sat) and VCE(sat) of transistor with temperature. **(2×10)**