

[Total No. of Questions - 9] [Total No. of Printed Pages - 3]  
(2064)

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**B. Tech 6th Semester Examination**

**Computer Architecture (ECE)**

**EC-6001**

**Time : 3 Hours**

**Max. Marks : 100**

*The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.*

- Note :** (i) Attempt five questions in all, selecting one question from each of the sections A, B, C and D along-with all the subparts of the question in section E.  
(ii) All questions carry equal marks.  
(iii) Make suitable assumptions wherever needed.

**SECTION - A**

1. (a) Discuss the basic structure of computer hardware and software. What is the significance of using 2's complement notation for number representation in computer systems? (10)  
(b) Differentiate between 'Hardwired control' and 'Micro-programmed control' signals. Also discuss the merits and limitations of each. (10)
2. Using an appropriate example explain 'Booth's multiplication algorithm'. Also discuss hardware requirements of the algorithm. (20)

**SECTION - B**

3. Draw and explain any three 'Cache memory mapping schemes' taking main memory size as 32 blocks, 8 words per block and cache size 8 block frames. Also comment upon the salient features of each mapping scheme. (20)

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4. Discuss the concept of 'Virtual memory'. How address space is mapped into memory space in a virtual memory system? Using appropriate diagram show memory table for mapping a virtual address. (20)

### SECTION - C

5. Discuss in detail 'Input-output interface'. Differentiate between 'Isolated and 'Memory mapped I/O'. (20)
6. (a) What is the basic advantage of 'Priority interrupt' over a 'Non-priority system'? Is it possible to have a priority interrupt without a mask register? Discuss. (10)
- (b) Describe 'DMA controller'. Why does DMA have a priority over CPU when both request a memory transfer? (10)

### SECTION - D

7. (a) How does 'Instruction level pipelining' improve performance of a computing system? (5)
- (b) A linear pipeline processor executes a program of 15000 instructions with a clock of 25MHz. The instruction pipeline has five stages and one instruction is issued per clock cycle. Calculate the speed-up factor in using this pipeline as compared to an equivalent non-pipelined processor to execute this program. What are the efficiency and throughput of this pipelined processor? List the assumptions made if any. (15)
8. (a) What makes pipelining hard to implement? What is 'Dynamic pipeline scheduling'? (10)
- (b) Take examples to illustrate 'Structural hazards', 'Data hazards' and 'Control hazards'. (10)

**SECTION - E**

9. (a) Differentiate between 'Synchronous' and 'Asynchronous data transfer'.
- (b) What is 'Threshing'?
- (c) What are 'Bit Slice Processors'?
- (d) Write & explain the format of micro-instructions.
- (e) Discuss the ways with which computer buses can be used to communicate with memory and input-output
- (f) Differentiate between 'Low order' and 'High order memory interleaving'.
- (g) Describe briefly modes of transfer to and from peripherals,
- (h) What is 'Pipelining'? Explain 'Pipeline efficiency'.
- (i) Compare and contrast 'Cache memory' v/s 'Virtual memory'.
- (j) Differentiate amongst 'Indirect address', 'Relative address' and 'Indexed address' modes. (2×10=20)