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14676

B. Tech 4th Semester Examination

Electronic Logic Circuit Design (O.S.)

EC-4003

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all selecting one question each from sections A, B, C and D. Section - E is compulsory.

SECTION - A

1. (a) Design a code converter which converts BCD code into excess-3 code..

   (b) A 'MS' flip-flop has two inputs M and S. Input M behaves like a J and S behaves like the compliment of K-input of J-K flip-flop

   (i) Tabulate the characteristics table of the flip-flop.

   (ii) Tabulate the excitation table.

   (iii) Show that by connecting the two inputs together, one obtains a D flip flop. (10+10=20)

2. (a) Differentiate between sequential and combinational circuits. Explain the various classifications of switching circuits.

(b) Design a minimal, three output contact network to realize the functions shown below. Ten transfer contacts are sufficient.

$T1(w, x, y, z) = \Sigma(0, 1, 2, 4, 8)$

$T2(w, x, y, z) = \Sigma(3, 5, 6, 9, 10, 12)$

$T3(w, x, y, z) = \Sigma(7, 11, 13, 14, 15)$ (10+10=20)

SECTION - B

3. (a) Design a sequential circuit with two D flip flops, A and B, and one input x. When x = 0, state of the circuit is same. When x = 1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

(b) Design a Mod-10 asynchronous counter using JK flip flops. (10+10=20)

4. (a) Explain finite state model. What are the capabilities of finite state machine?

(b) For each of the machines shown in table 1 and 2, find a minimum state reduced machine containing the original one.

Table 1

PS	NS, z		
	I1	I2	I3
A	C, 0	E, 1	–
B	C, 0	E,–	–
C	B,–	C, 0	A,–
D	B, 0	C,–	E,–
E	–	E, 0	A,–

Table 2

PS	NS, z	
	x=0	x=1
A	B, 1	H, 1
B	F, 1	D, 1
C	D, 0	E, 1
D	C, 0	F, 1
E	D, 1	C, 1
F	C, 1	C, 1
G	C, 1	D, 1
H	C, 0	A, 1

(10+10=20)

SECTION - C

5. A sequential circuit has two inputs, x_1 and x_2, and two outputs z_1 and z_2, is to be designed so that z_i (for i=1,2) takes on the value 1 if and only if x_i was the input that changed last.

   (a) Find a minimum-row reduced flow table and a valid assignment.

   (b) Assuming that all inputs are available in an uncomplemented as well as complemented form, show a realization using NAND gates. (20)

6. What are the advantages of asynchronous sequential circuits? What are pulse mode circuits? With the help of example describe the designing of pulse mode circuit. (20)

SECTION - D

7. (a) Explain the methods to design hazard free asynchronous circuits.

   (b) What are advantages of modularity? What are the conditions for serial and parallel decomposition.

   (10+10=20)

8. Design a hazard free asynchronous sequential circuit with two input x1 and x2 and two outputs G and R, which is to behave in the following manner. Initially, both input and both outputs are equal to 0. Whenever G =0 and either x1 or x2 becomes 1, G turns on i.e. becomes 1. When the second input becomes 1, R turns on. The first input that changes from 1 to 0 turns G off. R turns off when G is off and either input changes from 1 to 0.

   (20)

SECTION - E

9. (a) What are Mealy and Moore type machines?

(b) Realize the given T flip flop from a D flip flop.

(c) Convert a D-FF into JK-FF.

(d) What are the limitations of finite state machine?

(e) Tabulate the excitation tables of JK and SR flip flop.

(f) With the help of example explain the term glitch.

(g) Draw the state diagram of modulo-8 binary counter.

(h) Write down the main steps for the synthesis of synchronous circuits.

(i) Design a 3-bit ring counter.

(j) Express the function Y= A+BC in Canonical POS form.

(2×10=20)