

[Total No. of Questions - 9] [Total No. of Printed Pages - 3]
(2064)

14731

B. Tech 6th Semester Examination

Parallel Computing

IT-6005

Time : 3 Hours

Max. Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt any five questions in all, selecting at least one question from each section. However, section E is compulsory.

SECTION - A

1. (a) Design an algorithm to find the maximum of n numbers in $O(\log n)$ time on an EREW-PRAM model. Assume that initially each location holds one input value. Also explain how you would make this algorithm processor time optimal. (10)
- (b) Explain the problems as well as supporting issues to develop truly scalable computer system. (10)
2. Let α be the percentage of a program code which can be executed simultaneously by n processors in a computer system. Assume that the remaining code must be executed sequentially by a single processor. Each processor has an execution rate of x MIPS and all processors are equally capable.
 - (i) Derive an expression for effective MIPS rate when using the system for exclusive exclusion of this program in terms of the parameters n , α , x .
 - (ii) If $n = 16$ and $x = 4$ MIPS, determine the value of α which will yield a system performance of 50 MIPS. (20)

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SECTION - B

3. Explain the applicability and restrictions involved using Amdahl's law, Gustafson's law and Sun and Ni's law to estimate the speedup performance of an n-processor system compared with that of a single-processor system. Ignore all communication overheads. (20)
4. Explain Memory-bounded speedup performance models. (20)

SECTION - C

5. Define the following basic terms associated with memory hierarchy design:
 - (i) Virtual address space
 - (ii) Page Fault
 - (iii) Cache blocks
 - (iv) Address mapping
 - (v) Hashing function
 - (vi) Hit ratio
 - (vii) Multilevel page tables
 - (viii) Memory replacement policies
 - (ix) Memory Latency
 - (x) Split caches. (10×2=20)
6. Consider a two-level memory hierarchy M1 and M2. The hit ratio is h. c1 and c2 be the costs per kilobyte, p1 and p2 are memory capacities and t1 and t2 are the access times respectively.
 - (i) What is the effective memory access time t_a of this hierarchy?

- (ii) Plot E vs. h for r = 2, 10, 30, 50 and 100 on grid paper.
- (iii) What is the required hit ratio h to make $E > 0.75$ if r = 100. (8+8+4=20)

SECTION - D

- 7. (a) Consider the interleaved execution of k programs in multi-programmed microprocessor using m wired-NOR synchronization lines on n processors. Prove that the degree of multiprogramming is $\leq (-n + \sqrt{n^2 + 4blnm}) / (2b)$ where m are number of barrier lines needed for a program, l are number of process created in program and b are number of processors allocated to program. (10)
- (b) Explain E-cube routing on 4-D hypercube with suitable example. (10)
- 8. There are many ways to solve the mutual exclusion problem based on different implementation schemes such as use of spin locks or Dekker's protocol. Describe the following schemes except following:
 - (i) Using Binary Semaphores.
 - (ii) Using Monitor called by processes competing for critical section. (10+10)

SECTION - E

- 9. Explain the following topics:
 - (i) Role of Compilers
 - (ii) Grain Scheduling
 - (iii) Taxonomy of MIMD Computers
 - (iv) Demand Driven Mechanism
 - (v) Crossbar Switch. (5×4=20)