

[Total No. of Questions - 9] [Total No. of Printed Pages - 4]
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1338

B. Tech 3rd Semester Examination

Digital Electronics (N.S.)

EC-211

Time : 3 Hours

Max. Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all, select one question from each sections A, B, C and D. Section E is compulsory.

SECTION - A

1. (a) A transmitter uses a single error correcting code for the message using even parity. The message received at the receiving end is 1110101. Check and correct the error. Assume the parity code is even. (4)
 - (b) Convert the following numbers into decimal:
 - (i) 100100111000.0111 (BCD)
 - (ii) $(11001101.111)_2$
 - (iii) $(CF.5)_{16}$
 - (iv) $(234)_5$(4)
 - (c) Simplify the expression:
 $Y(ABCD) = (\bar{A} + B)(A + B + D)\bar{D}$ (4)
 - (d) Perform the following subtraction using 2's compliment method:
 - (i) $(0011.1001) - (0001.1110)$
 - (ii) $(3F)_{16} - (5C)_{16}$(4)
 - (e) Represent the number $(+46.5)_{10}$ as a floating point binary number with 24 bits. The normalized fraction mantissa has 16 bits and exponent has 8 bits. (4)
2. (a) Determine the single error correcting code for the message code (11010). Assume parity code is odd. (4)

1338/2200

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- (b) Perform the following subtraction using 1's complement method: **(4)**
 (i) $(11010)_2 - (10000)_2$ (ii) $(1000100)_2 - (1010100)_2$
- (c) Simplify the following expression:
 (i) $Y(A,B,C) = ABC + \overline{A}\overline{B} + \overline{A}B\overline{C}$
 (ii) $Y(A,B,C,D) = ACD + \overline{A}BCD$ **(4)**
- (d) What is Gray code? Give the advantages of Gray code over binary code. Write the Gray code for 4 bit binary number. **(4)**
- (e) For the function given below
 $f = \overline{A}\overline{B}D + A\overline{B}\overline{C}D + BCD$
 (i) Express f in standard SOP form
 (ii) Realize f using NAND gates only **(4)**

SECTION - B

3. (a) Reduce the following function using K-map technique and implement using NOR gates.
 $Y(A,B,C,D) = \prod M(0,1,2,3,8,9,10,11,12,13)$ **(5)**
- (b) Minimize the following Boolean function using K-maps:
 $Y(A,B,C,D,E) = \sum m(0,1,5,6,9,13,14,17,21,22,25,29)$ **(5)**
- (c) Simplify the following Boolean function using Quine-McCluskey method.
 $Y(A,B,C,D) = \sum m(1,2,3,5,9,12,14,15) + d(4,8,11)$ **(5)**
- (d) Define the following parameters of logic families and give their typical values for a standard TTL gate:
 (i) Propagation delay (ii) Fan-out
 (iii) Noise margin (iv) Figure of merit **(5)**
4. (a) Reduce the following function using K-map technique and implement using NAND gates:
 $Y(A,B,C,D) = \overline{A}\overline{B}D + A\overline{B}\overline{C}D + BCD$ **(5)**

- (b) Simplify the following four variable Boolean function using Quine-McCluskey method.

$$Y(A,B,C,D) = \Sigma m(1,3,5,10,11,12,13,14,15) \quad (5)$$

- (c) Simplify the following functions:

$$Y(A,B,C,D) = \Sigma m(1,3,7,11,15) + d(0,2,4) \quad (5)$$

- (d) Explain interfacing of a TTL gate driving CMOS gates and vice versa. (5)

SECTION - C

5. (a) Implement a full adder using two 4:1 multiplexers. (5)
 (b) What is race around condition in J-K flip-flop? How it can be eliminated. (5)
 (c) Explain the working of asynchronous up-down counter. (5)
 (d) Explain the working of bidirectional shift register. (5)
6. (a) Implement the following functions using 3-to-8-line decoder:
 (i) $Y_0(A,B,C) = \Sigma m(0,1,5,6)$
 (ii) $Y_1(A,B,C) = \Sigma m(0,4,5,7)$ (5)
 (b) Draw the logic circuit of J-K flip-flop and T flip-flop. (5)
 (c) Explain the working of 4-bit synchronous counter. (5)
 (d) What do mean by register? Also explain its different types. (5)

SECTION - D

7. (a) What is the need of A/D and D/A converter? List all D/A converters and explain. (10)
 (b) Explain the following:
 (i) PLA (ii) Sequential memories (10)
8. (a) Give different specifications of A/D and D/A converters. (10)

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- (b) What do you understand by semiconductor memories? Give its classification and organisation. (10)

SECTION - E

9. (a) Divide the binary number 110111 by 11. (1)
- (b) Find decimal equivalent of $(01010011)_2$ binary number. (1)
- (c) Write the dual of the Boolean theorem $A*(B+C) = AB+AC$ (1)
- (d) A full adder can be implemented with half adders and OR gates. How many half adders and OR gates are required for a 4-bit parallel full adder without any initial carry? (1)
- (e) How many flip-flops required to build Mod-15 counter? (1)
- (f) The Q output of J-K flip-flop is 1. The output does not change when a clock pulse is applied. What will be the input J and K? (1)
- (g) Write the minimum number of NAND gates required to implement $A + \bar{A}\bar{B} + \bar{A}\bar{B}C$ (1)
- (h) Why does the ECL family have the lowest propagation delay of all logic families? (2)
- (i) Encode the $(1011)_2$ binary word into 7-bit even parity hamming code. (2)
- (j) What are the different types of hazards in asynchronous circuits? (2)
- (k) Explain the basic flip-flop circuit for R-S using NOR gates. (2)
- (l) What is the difference between truth table and excitation table? (2)
- (m) What do you mean by sign-magnitude representation? (2)
- (n) Determine the value of base $(193)_x = (623)_8$ (1)