[Total No. of Questions - 8] [Total No. of Printed Pages - 3]
(2124)

1625

M. Tech 1st Semester Examination

Design of Electronics System

EC-102

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : (i) Assume suitable data wherever necessary.

(ii) Attempt Any FIVE Questions.

1. (a) Explain the successive approximation ADC with a suitable diagram. Compare dual slope ADC and successive approximation ADC in terms of accuracy conversion speed and resolution. What is the resolution of 12 bit successive approximation ADC? (12)

   (b) What do you mean by hazard free asynchronous sequential circuits? (6)

   (c) How many comparators are required to design 12-bit flash type ADC? (2)

2. (a) Implement the following Boolean function with only one 4X I MUX

   $F(A, B, C, D)=\Sigma m(0,2,3,6,8,9,12,14)$ (10)

   (b) Design 24-bit comparator using six 7485 comparators in two levels. (10)

[P.T.O.]

3. (a) Explain the steps involved in programming of FPGA. (8)

   (b) List the application of PI.A. (4)

   (c) Realize EX-OR gate using only four NAND gates. Also realize Full-Adder circuit using only NAND gates. (8)

4. (a) Design a BCD to Excess-3 code converter and implement using suitable PI.A. (15)

   (b) Write the design procedure for synchronous counter. Also design MOD-5 ripple counter. (5)

5. (a) Carry out the following conversion:

   (i) Convert a SR-latch to T Flip-Flop

   (ii) Convert JK to SR flip-Flop (10)

   (b) Draw and explain the clocked SR Flip-flop in detail. (5)

   (c) Write notes on bounce elimination switches. (5)

6. (a) Write the design procedure for asynchronous counter. Also design MOD-6 ripple counter. (8)

   (b) Analyze the sequential circuit as shown in Fig. 1. (12)

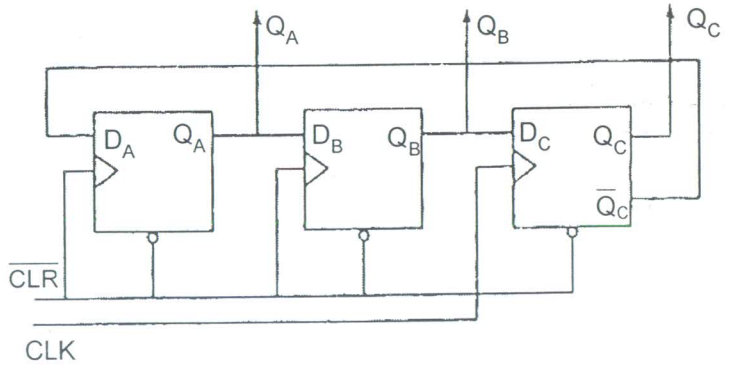

Fig. 1

7. (a) Explain the method to eliminate static hazards in asynchronous circuits with an example. (10)

   (b) Write notes on:

   (i) Electromagnetic Interference and Electromagnetic compatibility.

   (ii) Grounding and shielding of digital circuits. (10)

   (a) Design a 3-bit binary UP/DOWN counter with a direction control M. Use JK flip-Hops. (8)

   (b) Design a clocked sequential circuit for state diagram as shown in Fig. 2. (Use state reduction technique). Use D flip-flop. (12)

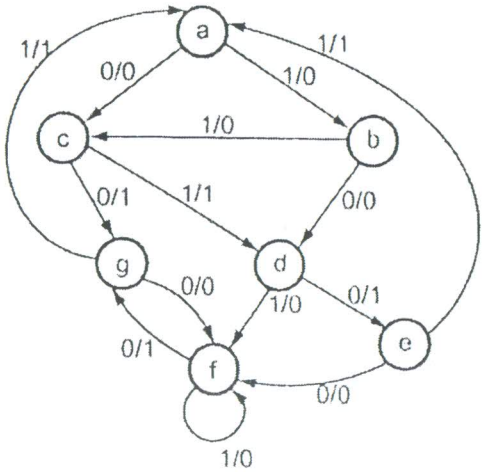

Fig. 2