[Total No. of Questions - 9] [Total No. of Printed ges - 3]
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B. Tech 3rd Semester Examination

Digital Electronics Engineering (NS)

EC-211

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : (i) Attempt five questions selecting one question from each section A, B, C and D.

(ii) Section E is compulsory.

(iii) Use of non-programmable calculator is allowed.

SECTION - A

1. (a) Convert the octal number $(765.43)_8$ into the binary, decimal and hexadecimal equivalent. (5)

   (b) Divide 110011_2 by 101_2. (5)

   (c) State and prove deMorgan's theorem for two variables. (5)

   (d) Generate the hamming code for the byte 10110010_2. (5)

2. (a) Convert the octal number $(257.46)_8$ into binary, hexadecimal and decimal numbers. (5)

   (b) Perform the subtraction using 2's complement arithmetic. (–52) – (–84). (5)

   (c) State and prove consensus theorem. (5)

   (d) Write short notes on error detection and correction codes. (5)

SECTION - B

3. (a) Reduce the following function using k-map. F(A,B,C,D,E) = Σ(0,2,3,8,11,10,15,17,22,24,30)+d(5,6,27,29,31). (10)

   (b) Draw a CMOS two input AND gate and two input OR gate. Explain each of its working. Derive the equations from the circuit. (10)

4. (a) Draw an ECL NOR gate and explain its working. Mention its advantages and disadvantages. (10)

   (b) Provide a circuit diagram which implements the following boolean function using only NAND gates F = (A + D'). (B + C + D').(A + B' + C') that has the don't care states: ABC'D', ABC'D, ABCD and ABCD'. (10)

SECTION - C

5. (a) Draw and explain the working of a BCD adder with the necessary equations (5)

   (b) Starting with a truth table, draw and explain the function of a 8:1 multiplexer (5)

   (c) Convert a J-K Flip Flop into D-FF and T-FF. Draw the necessary diagrams and derive the equations. (5)

   (d) Build a 4-bit binary ripple down-counter. Draw the circuit for the same (5)

6. (a) Draw and explain a 4-bit universal shift register. (5)

   (b) Construct a synchronous 4-bit BCD counter using D-FFs. Draw the circuit for the same. (5)

   (c) Draw the truth table of a full subtractor, derive the expressions and draw the circuit for the same. (5)

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(d) Explain the working of any encoder with suitable diagrams and equations. (5)

SECTION - D

7. (a) Draw and explain a DAC with binary ladder network. Discuss the pros and cons. (10)

   (b) Classify semiconductor memories. Describe PLAs and how logic is implemented on them with an example. (10)

8. (a) Write short notes on Content Addressable Memories. Draw necessary block diagrams. (10)

   (b) Draw and explain successive approximation ADC. (10)

SECTION - E

9. Each sub part carries 2 marks:

   (a) Rewrite the expression F=A+B+CD in canonical POS form.

   (b) Write the BCD equivalents of 8421 code.

   (c) Differentiate between RAM and ROM.

   (d) Draw the D-Latch and explain its working.

   (e) Draw a 4-bit asynchronous counter using T-FFs.

   (f) Convert the two's complement number $(1110)_2$ into its decimal equivalent

   (g) Write the truth table of a 2:4 Decoder and give its equation,

   (h) List the important parameters to be considered in an ADC.

   (i) Write the importance of parity and list some of its applications,

   (j) Differentiate between positive logic and negative logic. (10×2=20)