[Total No. of Questions - 9] [Total No. of Printed P ...s - 2]
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16098(D) - 0 DEC 2016

B. Tech 3rd Semester Examination

Digital Electronics (CBS)

EC-302

Time : 3 Hours **Max. Marks : 60**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt any one out of two questions in section A, B, C and D. All parts of section E are compulsory.

SECTION - A

1. (a) Perform subtraction on the following binary number using 2's compliments of the subtrahend. Where the result should be negative, 2's compliment it and affix a minus sign.

   (i) 100111-101101 (ii) 1001-110000

   (b) Determine Hamming code sequence with odd parity for 10011010 to make it an error correcting code. (10)

2. (a) Determine the base of number in each case for the following operation to be correct:

   (i) 302/20 =12.1 (ii) 24+17 = 40

   (b) Explain, positive and negative Logic in digital systems. (10)

SECTION - B

3. (a) Minimize the following function by using Karnaugh map and write the expression in product of sums:

   $F(a,b,c,d) = \Sigma(0,1,2,5,8,9,10)$

   (b) Design and realize 4 bits binary to Excess -3 code converter circuit by using minimum number of NAND gates. (10)

4. Draw and explain the logic circuit of Inverter and NAND gate using PMOS. (10)

SECTION - C

5. (a) Design a circuit for the conversion of S-R to J-k flip flop.

   (b) Write short note on Multiplexer and Demultiplexer and hence realize the following function using 4:1 multiplexer while connecting variable a and b to the select lines:

   $F(a,b,c,d) = \Sigma m(0,1,2,4,6,7,11,15)$ (10)

6. (a) Draw and Explain the circuit of J-K flip-flop.

   (b) Design a circuit for BCD to seven segments Decoder circuit. (10)

SECTION - D

7. (a) Design a 4-bit right shift register using j-k flip-flop.

   (b) Design a 3-bit asynchronous counter using j-k flip-flop. (10)

8. List the PLA programming table for the following two Boolean functions and implement in PLA:

   $F_1(a,b,c,) = \Sigma m\ (0,1,2,4)$

   $F_2(a,b,c,) = \Sigma m\ (0,5,6,7)$ (10)

SECTION - E (Compulsory)

9. Write short note on following:

   (a) Write the truth table of OR gate in negative logic.

   (b) Convert binary 1011 to Excess -3 code.

   (c) Define min and max terms.

   (d) What is race around condition?

   (e) Draw the excitation table of S-R flip-flop.

   (f) Draw and Explain the circuit of master slave J-K flip-flop?

   (g) What is the difference between Asynchronous and Synchronous sequential circuit?

   (h) What does SISO, SIPO, PISO and PIPO stands for?

   (i) Explain the difference between ROM and RAM?

   (j) Show that full adder circuit is a combination of two half adder circuit? (10×2=20)