[Total No. of Questions - 8] [Total No. of Pri d Pages - 2]
(2126)

16350(D)

M. Tech 3rd Semester Examination

Design of CMOS VLSI System

EC-307

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : (i) Attempt any five questions.
(ii) All questions are of equal marks.

1. (a) Describe the basic principle of MOS transistor. Explain the inversion layer formation in the N-MOSFET with the energy band diagram. Also explain why the bending of Fermi level is not possible. (10)

   (b) Describe and find out the threshold voltage for MOSFET device. Calculate the V_T for the Si n-channel MOSFET for gate to substrate work function difference Φms = 1.5eV, gate oxide thickness=100A°, accepter doping concentration in the bulk is $10^{18}cm^{-3}$ and fixed oxide charges of $5*10^{10}$ qC/cm^2, for a substrate bias of –2.5V. At V_T what are the electron and hole concentrations at oxide-Si interface? (10)

2. (a) What are reasons for short circuit current in CMOS? Derive the expression for short circuit power dissipation. (10)

   (b) Derive the rise time and fall time of CMOS inverter circuit. What is the essential condition for a symmetric inverter? (10)

3. (a) Design a multiplexer circuit using Ratioed logic, pass transistor logic and dynamic logic. (10)

   (b) What are the basic rules to draw the layout of CMOS circuits? Draw a transistor-level circuit diagram of a 2-input NAND gate in CMOS and describe its operation. Sketch a stick diagram and physical layout for the same gate, paying attention to the dimensions of the transistors to ensure balanced rise and fall times. (10)

4. (a) Explain the gate level schematic of clocked NOR based JK latch circuit and CMOS AOI realization of the JK latch. (10)

   (b) Describe the circuit and performance of CMOS Schmitt trigger circuit. (10)

5. (a) Elaborate various timing constraints on the clock frequency. Explain various factors affecting clock skew in the VLSI chips. Explain the H-tree clock distribution network. (10)

   (b) Explain the interconnect delay. Derive expression for effective resistance and capacitance estimation using RC delay model. What are various methods to mitigate the interconnect delay? (10)

6. (a) What are the SPICE basics for circuit simulation and power analysis? What are various types of transition modeling and analysis? (10)

   (b) Discuss transistor and interconnect scaling in detail. (10)

7. (a) Explain BJT structure and its operation. (10)

   (b) Sketch a transistor-level design and give a brief description of the method of operation for each of the following memory cells:
   (i) a dual-ported, static memory cell.
   (ii) a dynamic memory cell for dense memory.
   Explain the comparative merits of the three designs and explain where they might be used. (10)

8. Explain the following:
   (i) Figure of merits for low power VLSI design.
   (ii) TSPC dynamic Flip Flop.
   (iii) BiCMOS Applications.
   (iv) Domino CMOS Logic. (4×5=20)