[Total No. of Questions - 9] [Total No. of Printed Pages - 2]
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16218(D) - 0 DEC 2016

B. Tech 7th Semester Examination

Microelectronics Technology (NS)

EC-411(a)

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : (i) Attempt five questions in all selecting one question each from sections A, B, C and D. Section E is compulsory.
(ii) All Parts of a question should be answered at one place.
(iii) Answers should be brief and to the point and be supplemented with neat sketches.

SECTION - A

1. (a) Discuss the role of cleaning and etching in the growth of single silicon crystal.

   (b) Describe the mechanism to control the pull rate during the CZ crystal growth process. Also explain the float zone method for crystal growth. (8+12=20)

2. Explain the difference between evaporation and sputtering technology. Compare the magnetron sputtering and reactive sputtering in detail. (20)

SECTION - B

3. Derive the fick's first law explaining each step in detail in the context of Diffusion Process. Also explain how fick's law play its role when two miscible liquids are brought into contact with each other for diffusion to take place. (20)

4. (a) Write notes on Liquid phase epitaxy and vapour phase epitaxy.

   (b) Discuss the effect of the impurities of water and sodium on the oxidation rate during the process of thermal oxidation. (12+8=20)

SECTION - C

5. (a) How are ions selected in an implanter?

   (b) How is doping controlled (Measured) in an ion implantation process? (8+12=20)

6. (a) Discuss optical Lithography in detail.

   (b) What are the properties of the plasma? Explain the plasma assisted deposition of Silicon dioxide in IC fabrication. (12+8=20)

SECTION - D

7. (a) Which metal is mostly used for metallisation and why? Discuss the process of multilayer metallization for integrated circuits,

   (b) Discuss the various limitations of the metal aluminium used for the metallisation process. (12+8=20)

8. (a) Describe the N-Well Process for CMOS Fabrication in Detail.

   (b) Discuss the concept of CMOS Logic Gates. (15+5=20)

SECTION - E

9. (i) What is the role of spill tray in the set up of czochralski crystal puller?

   (ii) Differentiate physical vapour deposition and chemical vapour deposition.

   (iii) Explain the role of Meissner trap in PVD evaporation chamber.

   (iv) Give any two examples of epitaxial growth.

   (v) Discuss any two properties of oxide layer on silicon.

   (vi) Why mobile ionic charge is induced during the oxidation process?

   (vii) What is transverse straggle?

   (viii) What is channelling?

   (ix) Why throttle valve is used in the metallisation process?

   (x) How environment is affected by the power dissipation of VLSI circuits? (10×2=20)